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High Performance ASIC Design: Using Synthesizable Domino ...

High Performance ASIC Design: Using Synthesizable Domino Logic in an ASIC Flow Presenting methodologies for high speed ASIC design developed over several years in industry, this practical book covers issues related to the use of domino logic in

an automated framework, and brings together all the knowledge needed to apply them in practice.

High Performance ASIC Design: Using Synthesizable Domino ...

Accelerate your AI and machine learning applications with ASIC-based solutions from Socionext. Today's server, storage and networking equipment requires advanced, high-performance ASICs. As these custom chips become more complex, development typically becomes more challenging and time-consuming. When it comes to finding the right ASIC design for your AI and machine learning applications, Socionext offers turnkey, customizable solutions backed by an impressive track record of outstanding ...

High-Performance and Custom ASIC (SoC) | Socionext US

high-performance ASIC design, in the world. First-pass success

through automatic placement, routing, and checking has been achieved in many designs with the help of our design planning. Hierarchical Design Planner (HDP") environment. The key features implemented in HDP to meet the sub-half- micron design challenges include

Design planning for high- performance ASICs

Application-specific integrated circuit (ASIC) signal processors are necessary to achieve the high performance and low power requirements of modern applications, but long development times are one hurdle contributing to their declining adoption. ... %0 Thesis %A Bailey, Steven %T Rapid ASIC Design for Digital Signal Processors %I EECS ...

Rapid ASIC Design for Digital Signal Processors | EECS at ...

The design of application-specific integrated circuit (ASIC) is at

the core of modern ultra-high-speed transponders employing advanced digital signal processing (DSP) algorithms.

800G DSP ASIC Design Using Probabilistic Shaping and ...

A superior architecture is required to achieve high-performance, such as stability, low noise, high PSRR, and fast transient response, when designing capless LDOs. Vidatronic's Power Quencher ® LDO technology can be integrated onto the die and does not require an output capacitor.

Analog and Power Management Trends in ASIC and SoC Designs

Although an initial investment is required to develop an ASIC, the payoff for this investment is very high. Aside from a possible performance enhancement, a product using an ASIC requires fewer electronic components and is much cheaper to assemble. Having fewer parts translates into higher reliability overall.

What is an ASIC, and why is everyone using them? - Sigenics

Full-custom design is used for both ASIC design and for standard product design. The benefits of full-custom design include reduced area (and therefore recurring component cost), performance improvements, and also the ability to integrate analog components and other pre-designed —and thus fully verified—components, such as microprocessor cores, that form a system on a chip .

Application-specific integrated circuit - Wikipedia

Power consumption of ASICscan be very minutely controlled and optimized using many approaches such as Design Space Exploration DSE. ASIC is well suited for very high-volume mass production. ASICare...

Explained: ASIC Physical Design Flow | by Abhay Pawar ...

This paper presents a back-end design flow for high performance asynchronous ASICs using single-track full- buffer (STFB) standard cells and industry standard CAD tools to perform schematic capture, simulation, layout, placement and routing. This flow is demonstrated and evaluated on a 64-bit asynchronous prefix adder and its test circuitry.

High Performance Asynchronous ASIC Back-End Design Flow ...

In many modern ASICs, the design of the package is as important as the design of the ASIC itself. MegaChips has extensive packaging experience, including: High-performance, flip-chip BGAs with ball counts in excess of 2000 balls, Multi-chip modules (MCMs) – multiple die in a single package

ASIC Advanced Packaging Technology

A dedicated ASIC will have a signicantly better power-performance product than a general purpose processor or regular fabrics such as FP- GAs. For designs that push the envelope of power and per- formance, ASIC technology remains to be the only choice.

Pushing ASIC Performance in a Power Envelope

The HAPS (High-performance ASIC Prototyping Systems) family of products provides an integrated and scalable hardware-software solution leveraged by design and verification teams to improve their ASIC design schedules and avoid costly device re-spins.

HAPS Prototyping Solutions - Synopsys

ASIC companies must be either very knowledgeable in high-speed SerDes integration or rely on their SerDes IP vendor to support them in their development. There are many areas of

ASIC development outside of the custom analog/digital placement into ASIC design that require this knowledge, such as substrate design, PCB board design, supply noise, timing analysis and so on.

Enabling Integration Success Using High-Speed SerDes IP

Front-end Design Kit. We offer a development environment using standard EDA tools as a SoC development environment for customers and a tool we created for improving design efficiency as a design kit. The front-end design kit, which is uniquely optimized by Socionext, enables the development of high performance, small chip size, low power LSIs.

Front End Design | Custom SoC | Socionext US

High-performance ASIC design : using synthesizable domino logic in an ASIC flow. [Razak Hossain] -- Presenting a methodology for using domino logic in an ASIC design flow

developed over several years in an industrial context, this text covers practical issues related to the use of domino logic in... Your Web browser is not enabled for JavaScript.